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PROCESS RESEARCH ON POLYCRYSTALLINE SILICON MATERIAL

(PROPSM)

QUARTERLY REPORT NO. 10

APRIL 1, 1983 - JUNE 30, 1983

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The JPL Flat-Plate Solar Array Project is sponsored by the U.S. Department of Energy and forms part of the Solar Photovoltaic Conversion Program to initiate a major effort toward the development of low-cost solar arrays. This work was performed for the Jet Propulsion Laboratory, California Institute of Technology by agreement between NASA and DOE.

BY

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DESCRIPTION OF PROJECT

The purpose of this program is to determine the mechanisms affecting the conversion efficiency of polycrystalline silicon solar cells and, once knowing these mechanisms, to develop solar cell fabrication processes that take full advantage of its potential as a photovoltaic material. The primary emphasis of this work is on large-grain polycrystalline silicon as supplied by Semix, Inc. However, the results of this work are generic and will be applicable to all polycrystalline silicon materials.

ABSTRACT

The investigation of the performance-limiting mechanisms in large-grain (greater than 1-2 mm in diameter) polycrystalline silicon was continued by measuring the illuminated current-voltage (I-V) characteristics of the mini-cell wafer set. The average short-circuit current on different wafers is 3 to 14 percent lower than that of single-crystal Czochralski silicon. The scatter was typically less than 3 percent. The average open-circuit voltage is 20 to 60 mV less than that of single-crystal silicon. The scatter in the open-circuit voltage of most of the polycrystalline silicon wafers was 15 to 20 mV, although two wafers had significantly greater scatter than this value. The fill-factor of both polycrystalline and single-crystal silicon cells was typically in the range of 60 to 70 percent; however several polycrystalline silicon wafers have fill-factor averages which are somewhat lower and have a significantly larger degree of scatter. Lower average values of open-circuit voltage and a greater degree of open-circuit voltage and fill-factor scatter were correlated with the presence of inclusions, which was also correlated with significantly greater values of shunt conductance. Therefore, the scatter in the open-circuit voltage, fill-factor and power of solar cells presently fabricated from cast large-grain polycrystalline silicon is due, to some extent, to inclusions, which act as resistive shunts. However, this defect is not

intrinsic since a number of polycrystalline wafers shown no indication of excessive shunt conductance or the presence of inclusions.

Two processes, gettering and hydrogenation, are being investigated for improving the performance of polycrystalline silicon. Several experiments were performed to evaluate the usefulness of a 1000°C back-side damage-gettering heat treatment for removing minority-carrier lifetime-killing impurities. At present, no improvement in minority-carrier lifetime has been observed. The photoconductivity decay time of the polycrystalline silicon wafers was systematically and significantly degraded by longer heat-treatments at 1000°C. There appears to be a minority-carrier lifetime-killing mechanism in polycrystalline silicon that is activated by the high temperatures employed in this particular damage-gettering heat treatment.

A system for DC plasma hydrogenation of 2cm x 2cm samples is being refurbished to investigate grain and subgrain boundary passivation.

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I. INTRODUCTION

This report summarizes the progress achieved during the fifth quarter of a program to determine the mechanisms affecting the conversion efficiency of polycrystalline silicon solar cells and, once knowing these mechanisms, to develop solar cell fabrication processes that take full advantage of its potential as a photovoltaic material.

Section II of this report summarizes the results we have obtained by fabricating an array of small (approximately 0.2cm^2) photo-diodes across several 10cm x 10cm wafers. The illuminated current-voltage (I-V) characteristics of each wafer are summarized. Further analysis of the shunt conductance was performed and is also reported in Section II.

Two processes, gettering and hydrogenation, are currently being investigated for improving the performance of polycrystalline silicon. In Section III the results of several experiments on damage-gettered polycrystalline silicon wafers are described. A system for DC plasma hydrogenation of 2cm x 2cm samples is being refurbished to investigate grain and subgrain boundary passivation.

The conclusions to date on the mechanisms limiting the performance of polycrystalline silicon as a solar cell material are summarized in Section IV. Finally, the appendix contains a paper that was presented at the Symposium on "Materials and New Processing Technologies for Photovoltaics" of the 163rd Meeting of the Electrochemical Society. This paper describes the results and conclusions obtained from the thickness-resistivity matrix work that was performed earlier in this contract.

II. PROCESSES LIMITING THE PERFORMANCE OF POLYCRYSTALLINE SILICON MATERIAL

A. Mini-Cell Wafers

During the previous quarter a set of mini-cell wafers was fabricated, and measurements of their electrical characteristics were begun [1]. Three of the polycrystalline silicon wafers were from the central portion of Semix ingot 71-01E, from near the bottom, in the middle, and near the top of the brick. Two additional Semix wafers were from the middle of bricks C4-108 and C4-116B. A Wacker Silso wafer was processed, and a single-crystal silicon wafer was included as a control. Junction capacitance measurements showed that the boron concentration (resistivity) did not vary significantly with position, whether the wafer was from Semix or Wacker. Measurement of the shunt conductance of each mini-cell was used to locate areas of each

wafer where additional electrical and electro-optical measurements would not be influenced by the effects of a resistive shunt.

A test block for testing individual mini-cells with a Solarex solar simulator was designed and built. This simulator is normally used to test $4cm^2$ solar cells. An additional optical port was added for the mini-cell test block. Part of the test system for the $4cm^2$ cells consists of a DEC 11/03 mini-computer interfaced to the electronic load and to the cell test block. Solarex-developed software controls the test procedure and writes the current-voltage (I-V) characteristics of each tested cell onto an 8" magnetic floppy disk for permanent storage. A second DEC 11/02 minicomputer off-line is used to read the data-file disk, analyze the I-V data, and generate reports, again using Solarex-developed software.

Work this quarter consisted of interfacing the computer to the mini-cell test block, modifying the existing Solarex-developed cell testing software for use with the mini-cell wafers, measuring the mini-cell wafers, and writing software to list and analyze this data. The cells were tested under an AM0, 135 mW/cm^2 light source at $25^{o}C$.

The mini-cell test program measures and stores the AM0, red-filtered (Corning filter 2408), and blue-filtered (Corning filter 9788) I-V curves (40 current-voltage points) and characteristics (such as short-circuit current, open-circuit voltage, peak power, and fill-factor), plus the junction capacitance and shunt conductance of each mini-cell, which is given a unique wafer and location label. Each data disk is capable of storing the I-V data from 1450 mini-cells, that is, all of the data from about four 10cm x 10cm mini-cell wafers.

Software for listing the data was written and was used to begin evaluating the data. Cells that were not isolated (due either to incomplete mesa etching or to silver shorting the mesa isolation) and cells that were cracked were removed from the data. In general, the number of cells that were unusable due to processing problems was not excessive. Overall, about 60 to 80 percent of the cells from each wafer had no obvious processing defect. The average, standard deviation, coefficient of variance, and range of the characteristics for each wafer are shown in Table 1.

The average short-circuit current density (J_{sc}) of the polycrystalline cells was always less than that of the single-crystal control wafer (SC11-1). In the best material (C4-116B), the difference was only 3 percent; the bottom wafer of brick 71-01E was about 14 percent lower. The scatter for the wafers

WAFER		J_{sc} (mA/cm^2)	V_{oc} (mV)	P_p (mW/cm^2)	FF (%)	J_R (mA/cm^2)	J_B (mA/cm^2)	G_S (mmho/cm^2)	ρ (ohm-cm)
SC11-1	AVG	30.3	580	10.9	61.7	16.3	8.5	1.78	1.14
	STD DEV	0.4	15	1.0	4.2	0.2	0.2	2.85	0.07
241 CELLS	COEF VAR	1.3	2.6	9.0	6.9	1.5	2.2	-	6.2
	RANGE	29.2-31.0	500-598	7.4-12.2	45.3-68.2	15.8-16.7	7.5-8.9	0.01-23.55	0.93-1.44
71-01E/TOP	AVG	27.9	562	10.5	66.3	14.6	8.2	1.85	1.51
	STD DEV	0.6	16	1.1	5.7	0.4	0.1	4.58	0.11
294 CELLS	COEF VAR	2.1	2.9	10.8	8.6	2.9	1.6	-	7.1
	RANGE	26.3-29.3	512-583	3.5-11.9	46.0-73.3	12.8-15.4	7.7-8.6	0.00-55.91	1.13-1.87
71-01E/MID	AVG	27.9	560	10.6	63.9	14.6	8.0	6.83	1.56
	STD DEV	0.8	19	1.4	7.2	0.5	0.2	13.02	0.15
255 CELLS	COEF VAR	2.8	3.4	13.6	11.2	3.4	2.7	-	9.5
	RANGE	25.9-30.3	414-585	3.6-11.9	29.6-73.7	13.6-15.6	7.1-8.6	0.01-90.83	0.57-1.87
71-01E/BOT	AVG	26.1	520	7.7	55.5	13.2	7.9	10.02	1.70
	STD DEV	0.5	42	1.7	9.6	0.3	0.2	15.70	0.13
271 CELLS	COEF VAR	2.0	8.1	22.4	17.2	2.5	2.5	-	7.5
	RANGE	24.0-27.6	263-554	1.9-10.1	28.4-70.4	11.8-14.0	7.0-8.3	0.00-100.80	0.98-2.02
C4-116B	AVG	29.4	559	10.6	64.6	15.2	8.7	1.51	2.24
	STD DEV	1.6	14	1.0	3.3	1.2	0.2	2.40	0.15
329 CELLS	COEF VAR	5.6	2.5	9.3	5.2	7.9	1.9	-	6.5
	RANGE	26.2-31.9	522-588	8.0-12.3	50.4-70.2	12.9-17.0	8.2-9.2	0.00-19.24	1.80-2.60
C4-[illegible]8	AVG	28.1	540	8.9	56.9	14.4	8.3	13.83	1.69
	STD DEV	1.9	55	2.4	11.0	1.2	0.4	20.77	0.10
287 CELLS	COEF VAR	6.7	10.1	27.3	19.3	8.5	4.4	-	6.0
	RANGE	15.2-30.9	169-586	1.1-12.7	26.0-71.2	10.7-16.4	6.5-9.0	0.00-154.09	1.51-1.8
WACKER	AVG	27.5	551	9.7	63.6	14.0	8.3	3.31	1.61
	STD DEV	0.8	14	1.0	5.2	0.7	0.2	4.82	0.12
308 CELLS	COEF VAR	2.7	2.6	10.2	8.1	4.7	2.2	-	7.2
	RANGE	25.4-29.6	434-582	3.4-11.2	36.2-70.9	12.0-17.6	7.8-9.7	0.00-41.90	1.16-1.95

TABLE 1

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from brick 71-01E and for the Wacker wafer was less than 3 percent; the scatter in the short-circuit current of the wafers from brick C4-116B and C4-108 was significantly greater, 5.6 and 6.7 percent, respectively.

The average open-circuit voltage (V_{OC}) of the polycrystalline cells is about 20 to 60 mV lower than the average of the single-crystal control cells, which was 580 mV. The scatter for the cells from the top and middle wafer of brick 71-01E, from C4-116B, and from the Wacker wafer, is similar to that of the single-crystal control - about 15 to 20 mV. However, the cells from the bottom wafer of brick 71-01E and from the wafer from brick C4-108 have an open-circuit voltage scatter that is significantly greater - 42 and 55 mV, respectively. These two wafers also have cells whose average open-circuit voltage is significantly lower than that of the single-crystal controls or the other polycrystalline wafers.

With the exception of the wafers from the bottom of brick 71-01E and from brick C4-108, the average fill-factor (FF) of the cells from the remaining polycrystalline wafers and from the single-crystal control wafer are similar and do not show excessive scatter. The average fill-factor is low (62 to 66 percent) for these wafers, including the single-crystal control wafer, due to the series resistance resulting from the lack of a fine front grid metallization. The average fill factor of the

wafers from the bottom of brick 71-01E and from brick C4-108, 56 and 57 percent, respectively, is lower than that of the other wafers; in addition, their scatter is substantially greater.

As a result of the lower open-circuit voltages and lower fill-factors of the cells from the bottom wafer of brick 71-01E and from the wafer from brick C4-108, the average peak power (P_p) of these cells is also substantially lower than that of the other wafers.

The red-filtered short-circuit current density is sensitive to the minority-carrier diffusion length. The red filter transmits only these wavelengths longer than about 620 nm; this light would have an absorption coefficient in silicon of less than $4x10^3$ cm^{-1} and would be able to penetrate deeply into the bulk. Hence, carriers generated far from the junction by this long- wavelength light will be collected only if the minority-carrier diffusion length is sufficiently long. The blue filter transmits those wavelengths shorter than 600 nm. This light is able to penetrate only about 2 microns into silicon; therefore, the blue-filtered short-circuit current density is most sensitive to changes in the junction and near-junction regions.

The red-filtered short-circuit current density (J_R) of the polycrystalline cells is less than that of the single-crystal control cells, indicating shorter minority carrier diffusion

lengths in the polycrystalline silicon. The scatter in the red-filtered short-circuit current density of the cells from brick 71-01E is greater than that of the single-crystal control cells, but is substantially less than the scatter of the cells from the other polycrystalline wafers. The blue-filtered short-circuit current density (J_B) is fairly constant although it is somewhat greater for the single-crystal control wafer and the wafer from brick C4-116B.

The average shunt conductance (G_S) varies substantially from wafer to wafer and within each wafer. It is low, less than 2 mmho/cm^2, in the single-crystal control wafer, in the top wafer from brick 71-01E, and in the wafer from brick C4-116B. It is very high, greater than 5 mmho/cm^2, in the wafers from the middle and bottom of brick 71-01E and from the middle of brick C4-108. The average shunt conductance of the Wacker wafer is intermediate at 4.8 mmho/cm^2. Shunt conductance tends to increase from the top to the bottom of brick 71-01E. The ranges of the shunt conductance of the cells from the wafers from the middle and bottom of brick 71-01E and from brick C4-108 are 91, 100, and 154 mmho/cm^2, respectively, which are significantly greater than those of the remaining polycrystalline wafers (19 to 55 mmho/cm^2).

The average resistivity (ρ) of nearly all of the wafers is in the 1 to 2 ohm-cm range; the resistivity of the wafer from brick C4-116B is somewhat higher, which may account for the slightly greater short-circuit current density, due to a longer minority carrier diffusion length. There is no significant scatter in resistivity in any wafer; the resisitivity appears to be fairly uniform across any polycrystalline wafer, whether from Semix or Wacker, and whether from the top, middle or bottom of the brick. There is some indication that the resistivity is slightly higher, and the dopant concentration is slightly lower, at the bottom of brick 71-01E.

B. Shunt Conductance of Polycrystalline Silicon Wafers

Of particular interest in the data from the mini-cell wafers is the wide variation in shunt conductance of the mini-cells from wafer to wafer and, especially, within any wafer. The averge shunt conductance varies by more than an order of magnitude from wafer to wafer, from a low of 1.5 mmho/cm^2 for wafer C4-116B to a high of 20.8 mmho/cm^2 for C4-108. Shunt conductances on the order of 1 mmho/cm^2 have little effect on cell performance. However, shunt conductances greater than 10 mmho/cm^2 will reduce the theoretical fill-factor by more than 20 percent. Thus, shunt conductances that are consistently greater than 10 mmho/cm^2 are a serious impediment to achieving a high efficiency solar cell

Figures 1 through 7 show histograms of shunt conductance for each mini-cell wafer. The single-crystal wafer, Figure 1, shows a peak somewhere in the range of 0.2 to 5 mmho/cm^2. While this is not encouragingly low, it should be mentioned that this wafer was broken into two pieces during processing. Only about 1 percent of the cells from this wafer have values of shunt conductance greater than 10 mmho/cm^2.

Figures 2, 3 and 4 are for the top, middle, and bottom wafers, respectively, from Semix brick 71-01E. The top wafer has a nearly flat distribution from about 0.01 mmho/cm^2 to 10 mmho/cm^2. Interestingly, the peaks occur in the same ranges as in the single-crystal wafer, 0.2 to 0.5 mmho/cm^2 and 2 to 5 mmho/cm^2. The middle wafer, in contrast, has only one peak, at 2 to 5 mmho/cm^2, with a normal-looking distribution about the maximum. The distribution for the bottom wafer is skewed toward higher values of shunt conductance, with a maximum at 20 to 50 mmho/cm^2. There is also a peak at 2 to 5 mmho/cm^2. Only about 4 percent of the cells of the top wafer have values of shunt conductance greater than 10 mmho/cm^2. However, more than 18 percent of the middle wafer's cells, and nearly 30 percent of the bottom wafer's cells, have shunt conductances greater than 10 mmho/cm^2. Microscopic examination of these cells revealed that many inclusions were present in those cells with large shunt conductances.

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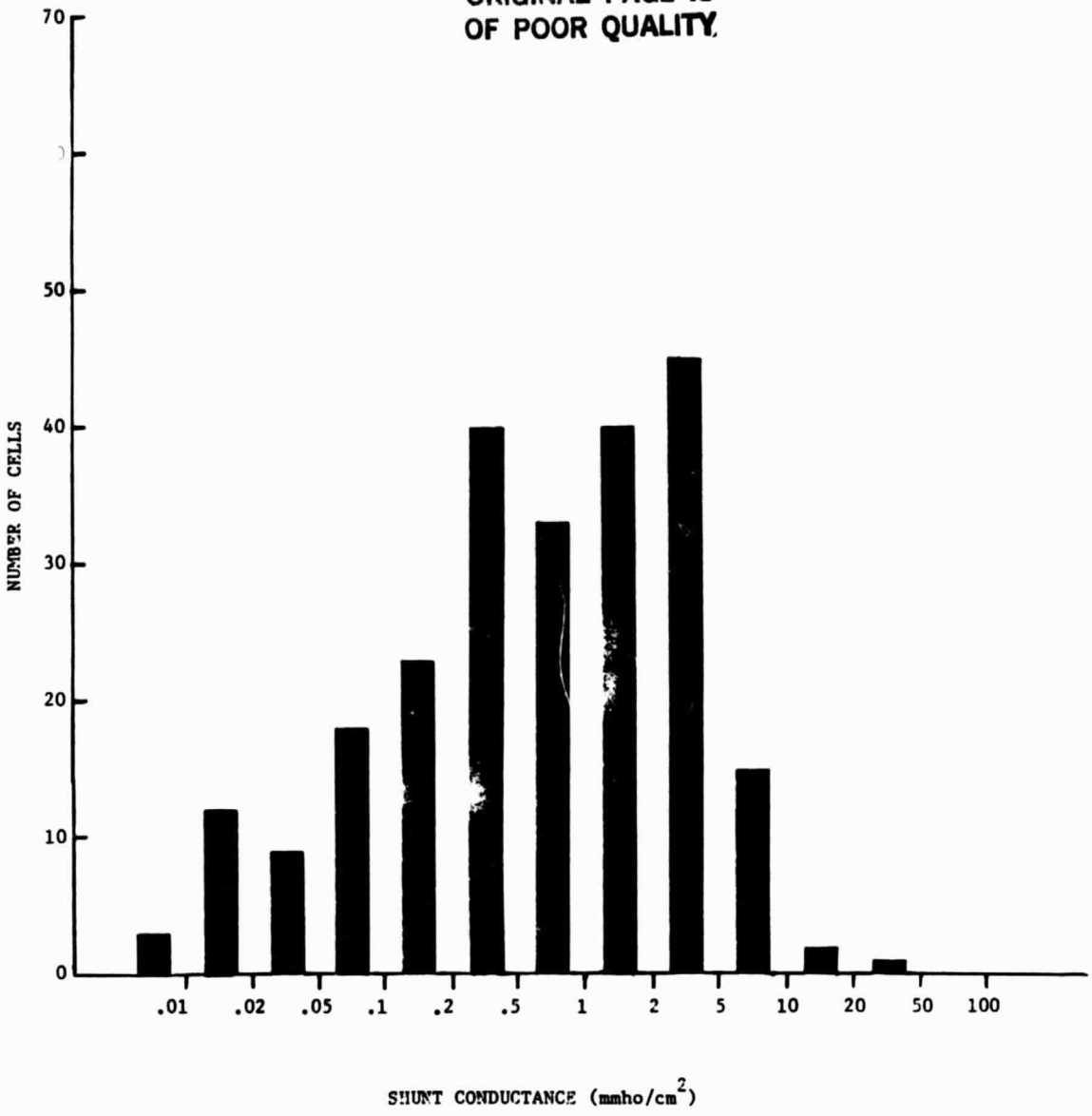

FIGURE 1. Histogram of shunt conductance for the single-crystal Czochralski wafer (SC11-1).

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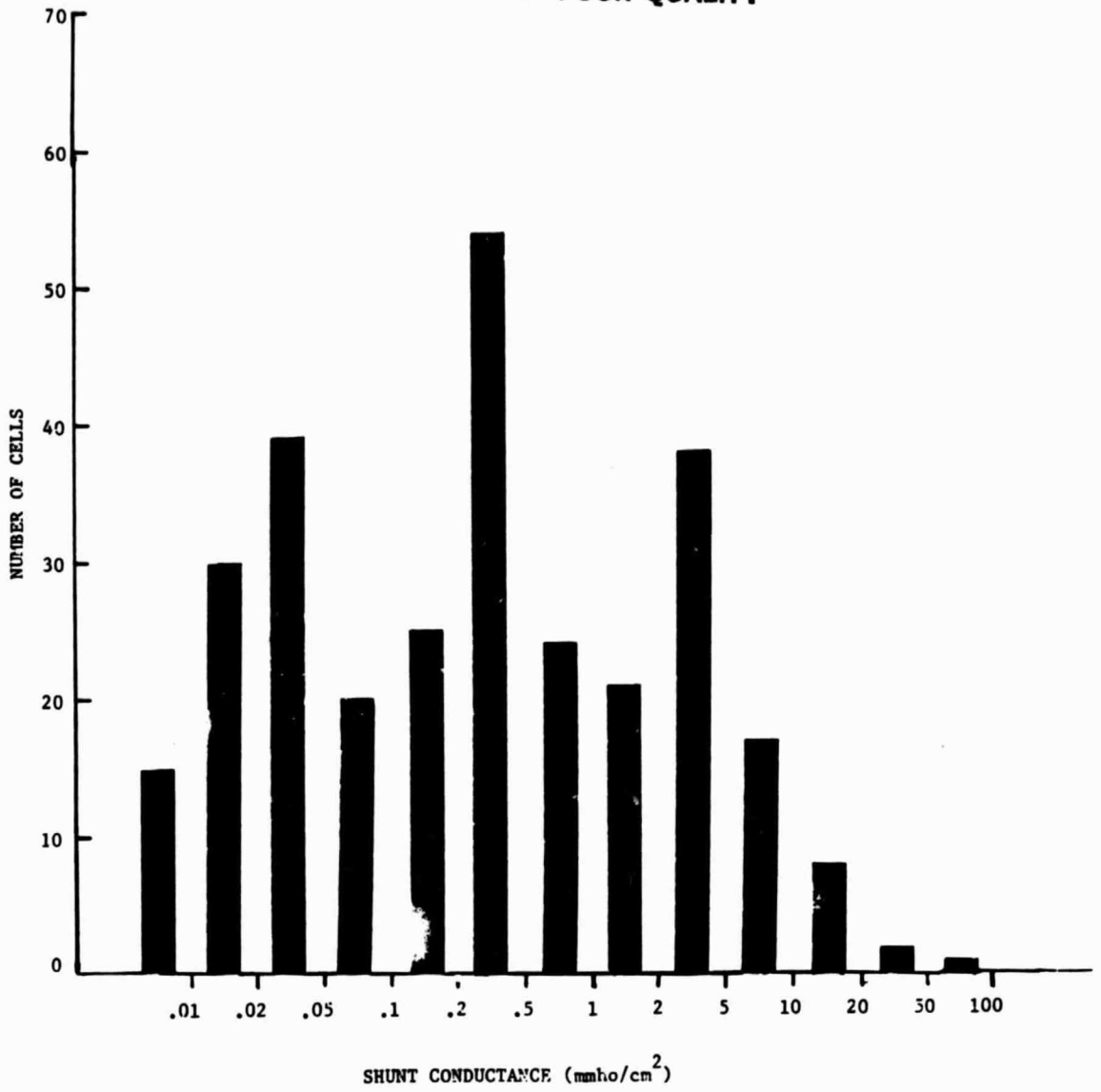

FIGURE 2. Histogram of shunt conductance for the top wafer from Semix brick 71-01E.

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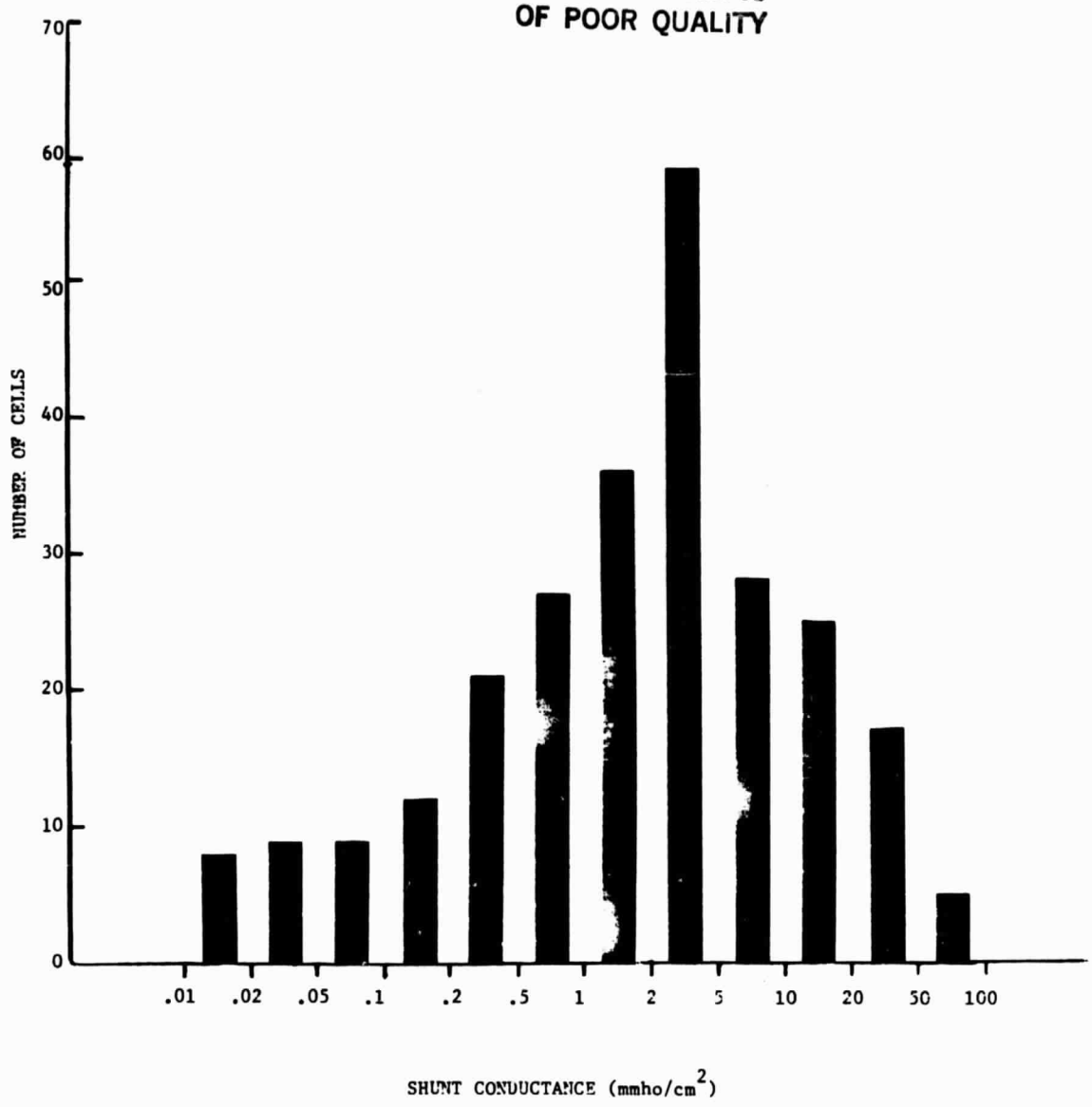

FIGURE 3. Histogram of shunt conductance for the middle wafer from Semix brick 71-01E.

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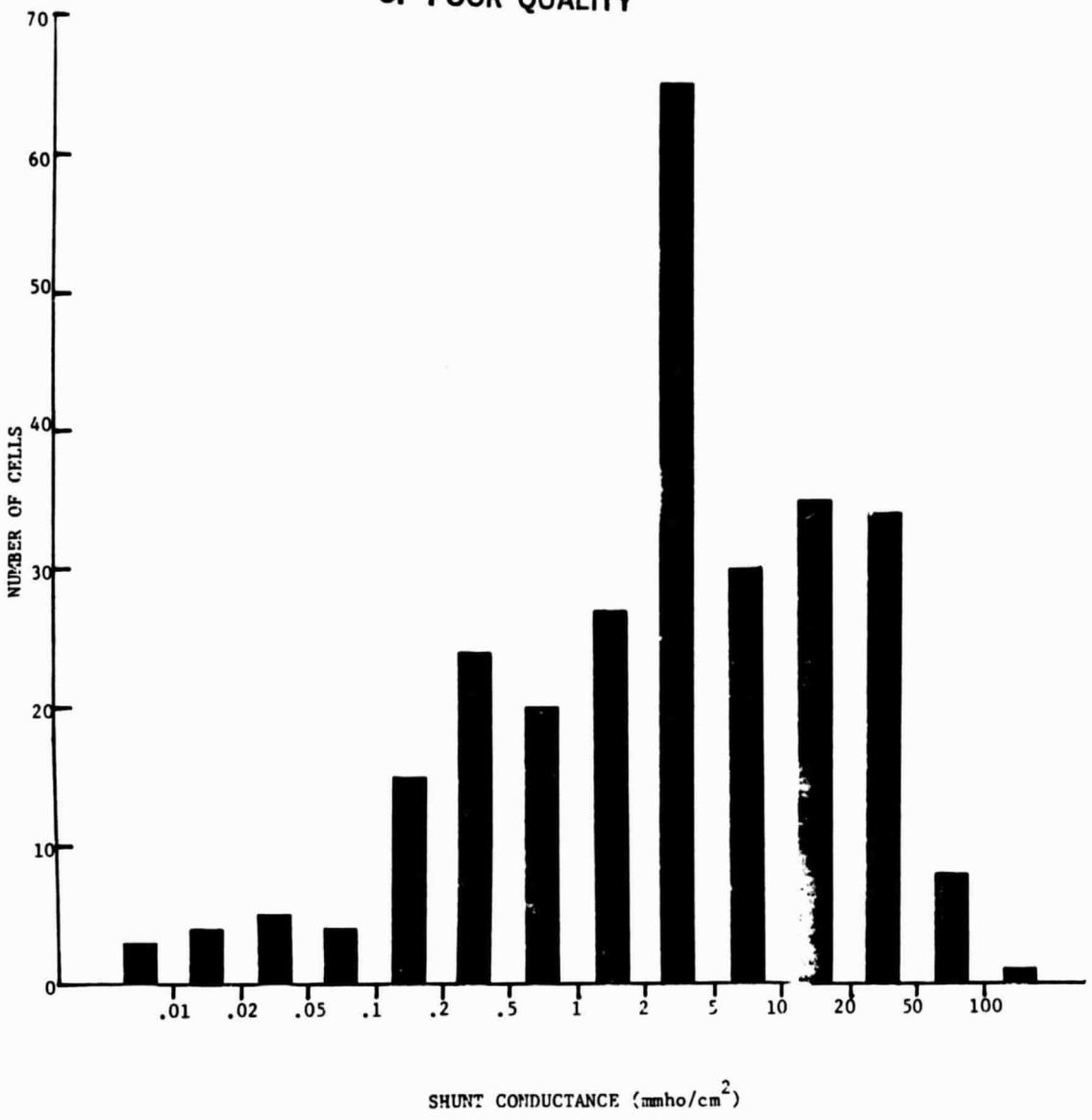

FIGURE 4. Histogram of shunt conductance for the bottom wafer from Semix brick 71-01E.

This observation was repeated with wafer C4-108, whose histogram, shown in Figure 5, has a peak at 10 to 20 mmho/cm^2 as well as 2 to 5 mmho/cm^2 and is skewed toward higher shunt conductances. About 40 percent of the cells have values of shunt conductance greater than 10 mmho/cm^2. Many inclusions were present in these cells.

In contrast, wafer C4-116B has a distribution, Figure 6, which, while skewed toward higher shunt conductances, has a peak in the 0.5 to 2.0 mmho/cm^2 range. Very few inclusions were observed in this wafer, and only about 1 percent of the cells had values of shunt conductance greater than 10 mmho/cm^2.

Finally, the distribution for the Wacker Silso wafer is shown in Figure 7. This is also skewed toward hugh shunt conductances with a maximum in the range of 2 to 5 mmho/cm^2. Some inclusons were present in this wafer. About 7 percent of the cells have values of shunt conductances greater than 10 mmho/cm^2.

While several interpretations of this data can be made, of significance is the fact that, for the wafer from the bottom of brick 71-01E and from brick C4-108, large numbers of high shunt conductance cells correlated strongly with the presence of many inclusions. These two wafers are also characterized by a large scatter in open-circuit voltage, peak-power, and fill-factor.

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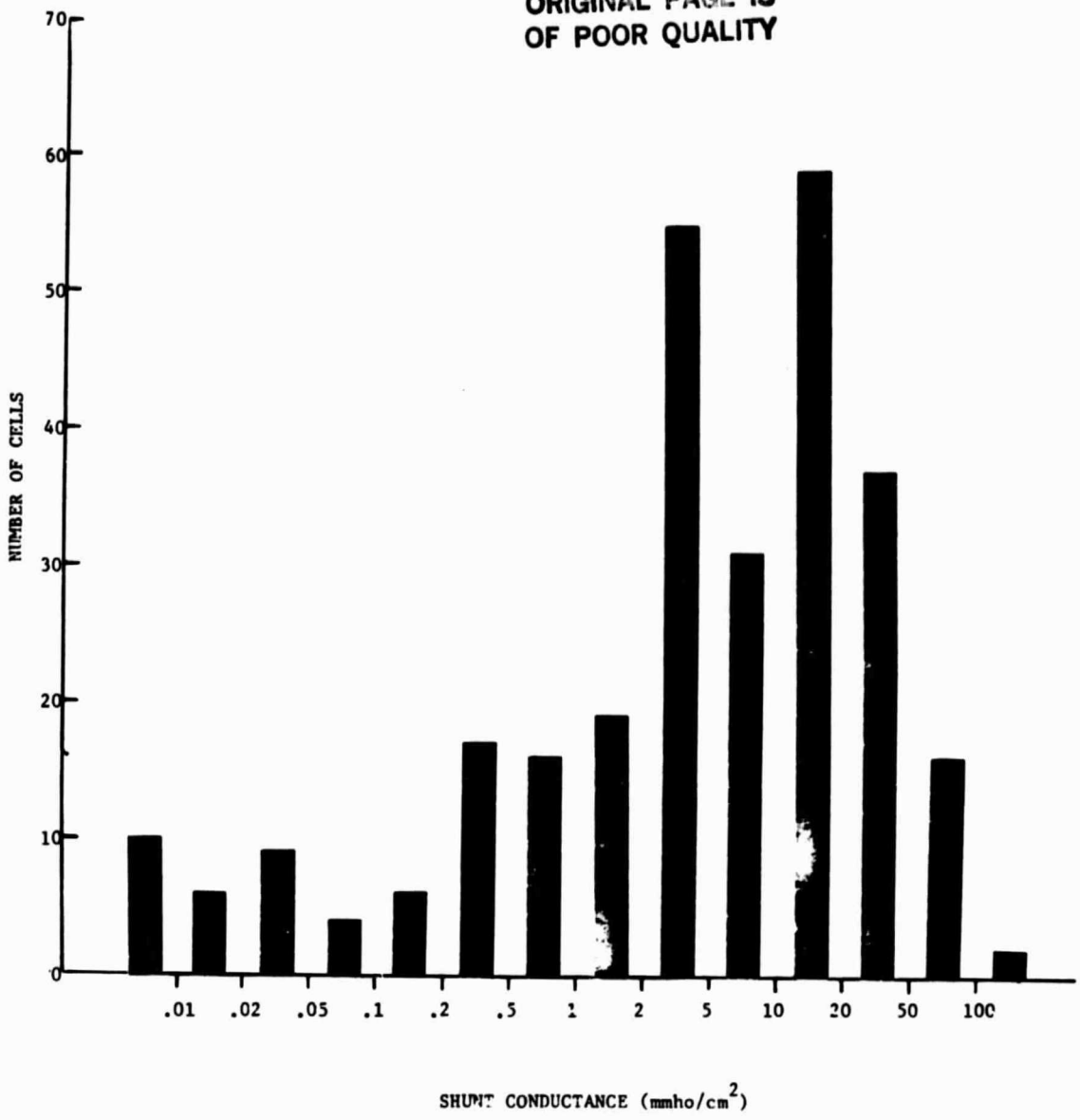

FIGURE 5. Histogram of shunt conductance for the wafer from Semix brick C4-108.

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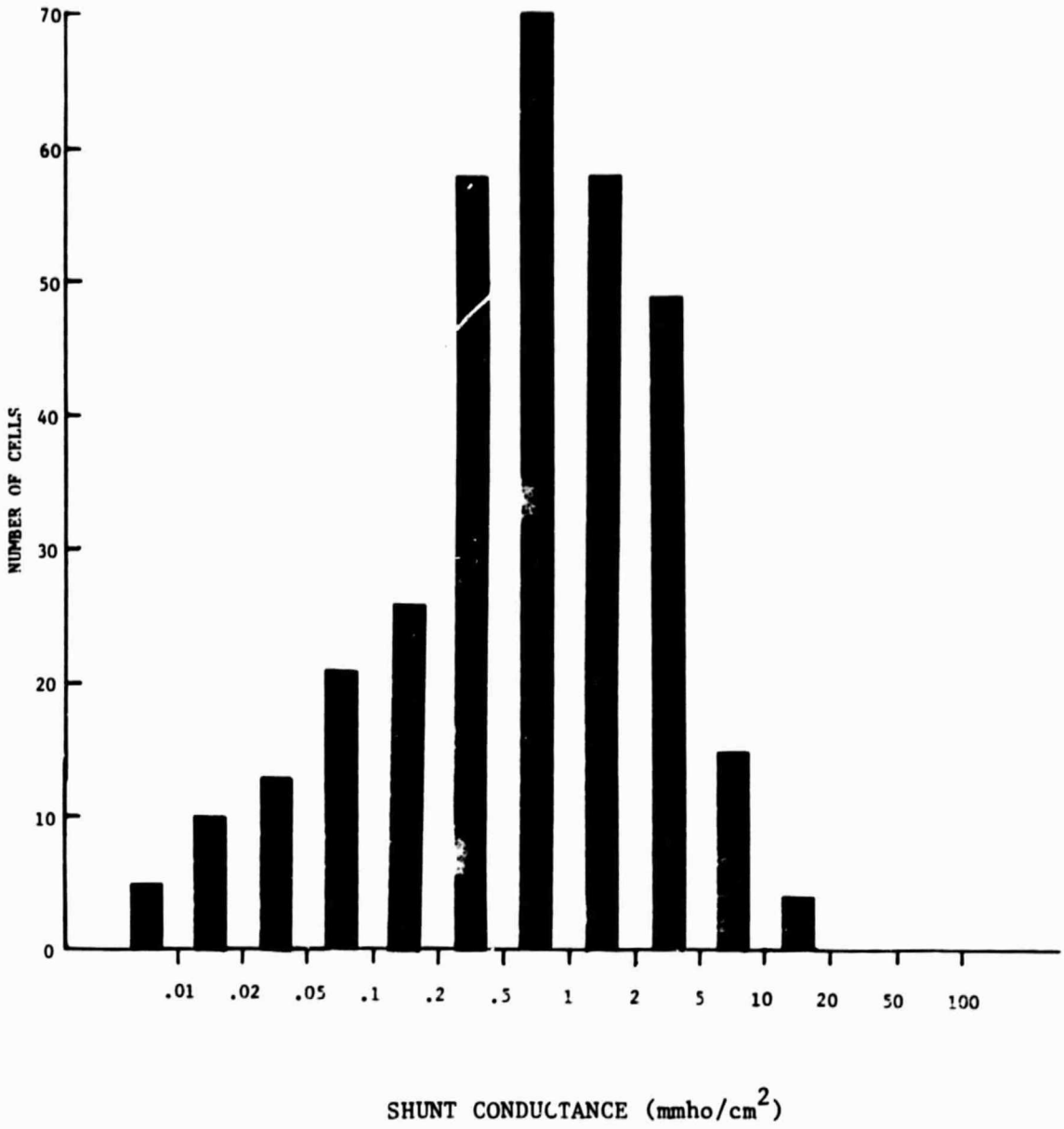

FIGURE 6. Histogram of shunt conductance for the wafer from Semix brick C4-116B.

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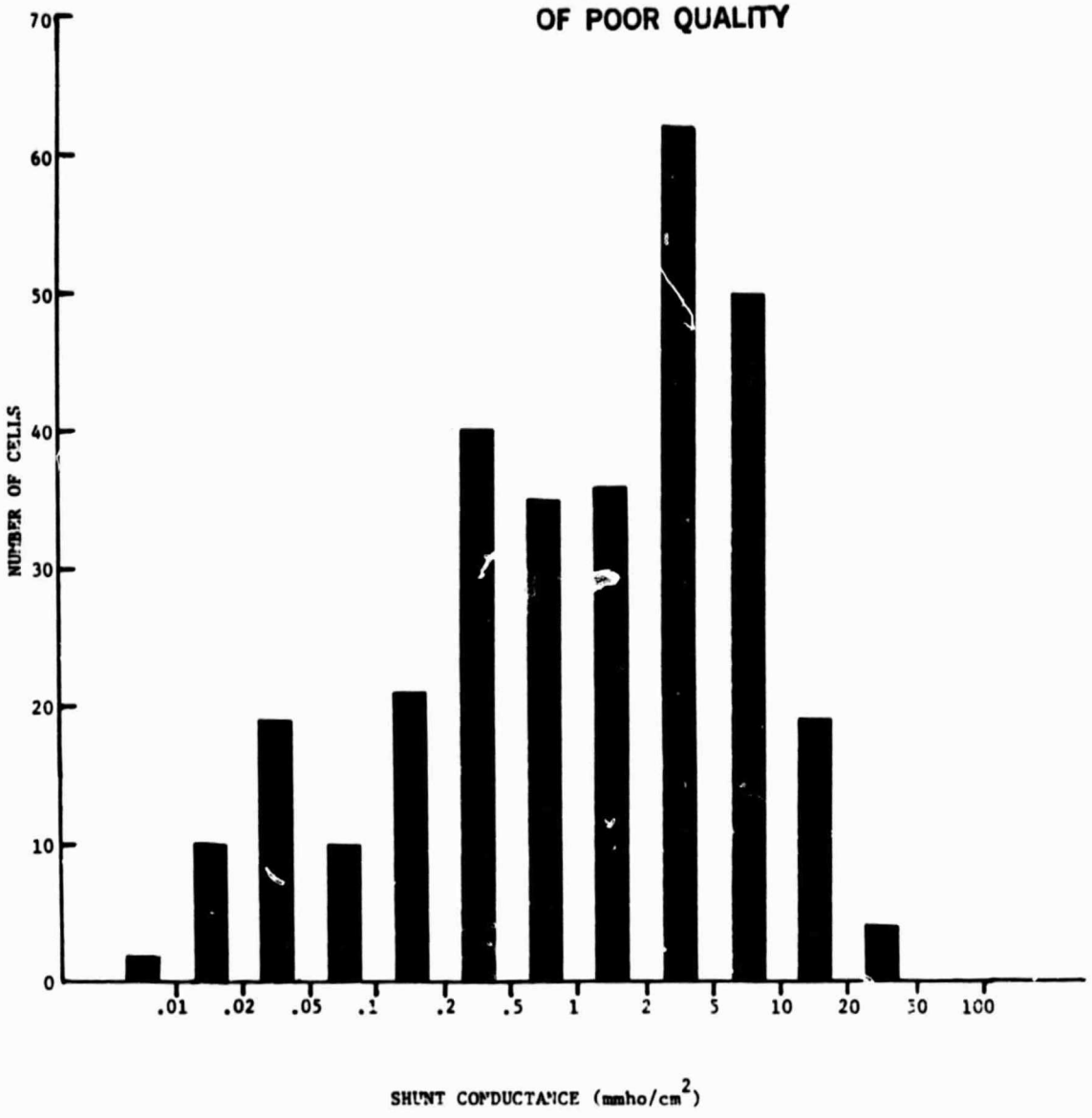

FIGURE 7. Histogram of shunt conductance for the Wacker Silso wafer.

Their short-circuit current, red-filtered current, and resistivity were fairly uniform. This implies that, to some extent, the scatter observed in the open-circuit voltage, fill-factor, and peak-power of cells presently fabricated from cast large-grain polycrystalline silicon is due to inclusions, which act as resistive shunts.

III. PROCESSES TO IMPROVE THE EFFICIENCY OF POLYCRYSTALLINE SILICON MATERIAL

A. Gettering

Results from the thickness-resistivity matrix indicated that polycrystalline silicon is presently characterized by a minority carrier diffusion length that is somewhat shorter than that of Czochralski single-crystal silicon. The cause of the shorter minority carrier diffusion lengths in polycrystalline silicon has not been unequivocally identified, but one possibility is that this reduction is due to a minority carrier lifetime-killing impurity. It may be possible, if indeed this is the case, to improve the short-circuit current of polycrystalline cells by removing some of this impurity, particularly if it is a fast-diffusing species, by a procedure known as damage gettering, which has been reported to result in a significant increase in minority carrier diffusion length in metallurgical grade silicon [2]. During this quarter a number

of experiments were performed to evaluate the effect of a 1000°C damage-gettering heat treatment upon the performance of large-grain polycrystalline silicon.

An experiment was performed to evaluate the cleanliness of the annealing tube. Four polycrystalline and four single-crystal silicon 5cm x 5cm wafers were etched using a CP etch to a thickness of 250 microns and then damaged using 320 mesh aluminum oxide powder to sand-blast the back side. The polycrystalline silicon was from Semix brick C4-87E. Each wafer was then cut in half. The left half was heat-treated at 1000°C for 25 hours in a fused quartz tube furnace under flowing nitrogen. The right half, the control, was not heat-treated. If the tube were contaminated with lifetime-killing impurities, or if the wafer handling technique were reducing the minority carrier lifetime, then this should be clearly shown by comparing a heat-treated single-crystal sample to its control.

The microwave reflectance photoconductivity decay technique was used to monitor the change, if any, in the minority carrier lifetime as a result of the heat-treatment. This technique has been previously shown [3] to be useful in determining the variation in an approximate value of minority carrier lifetime across a 10cm x 10cm polycrystalline silicon wafer since there was a strong correlation between the red-filtered short-circuit current (which is sensitive to minority carrier lifetime) of a

$4cm^2$ solar cell and the value of the microwave photoconductivity decay time constant of the silicon used to fabricate the cells, as shown in Figure 8. Therefore, this technique can be used, by measuring the photoconductivity decay time constant, to obtain an estimate of the minority carrier lifetime in the bulk material, assuming all conditions are similar. The exact relationship between the time constant and the minority carrier lifetime has not been determined, and the two are not necessarily equivalent. Because the photoconductivity decay time constant is sensitive to a number of intrinsic and extrinsic parameters, absolute values of time constant are not meaningful. However, if all test and sample conditions are maintained constant, the technique can be validly used to evaluate changes in minority carrier lifetime.

After the heat-treatments were completed, all samples were CP-etched to remove any surface damage and then lightly diffused in order to measure the microwave conductivity decay time constant. The photoconductivity decay time constant (hereafter, photoconductivity decay time) was evaluated at eight points on each 5cm x 5cm wafer using the technique described in Reference 2. The results of these measurements are shown in Table 2. The photoconductivity decay time of both the single-crystal and polycrystalline wafers decreased as a result of the heat treatment. However, while the photoconductivity decay time of the single-crystal silicon samples decreased by less than a

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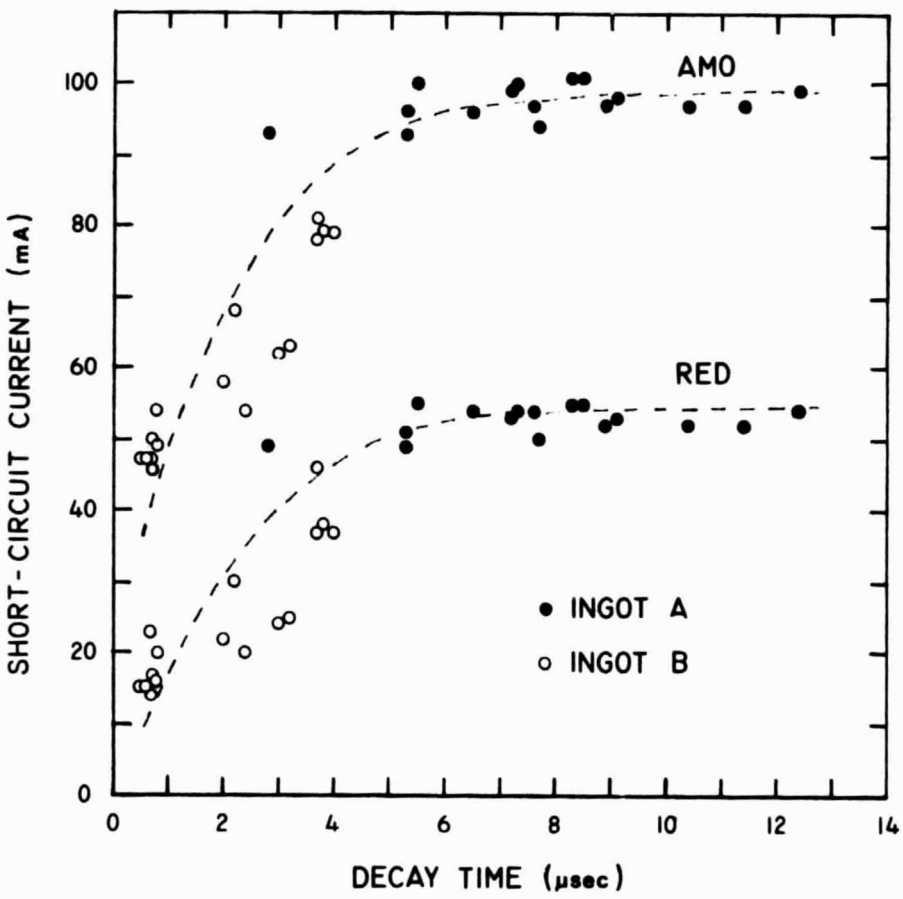

FIGURE 8. AMO and red-filtered short-circuit current as a function of photoconductivity decay time, using the technique described in Reference 3.

TABLE 2

Change in photoconductivity decay time constant (in μsec) due to 1000°C heat-treatment for 25 hours under flowing nitrogen.

SAMPLE	NO HEAT-TREATMENT	25 HOURS/1000°C
SINGLE-CRYSTAL - 1	6.2 ± 1.0	3.8 ± 0.4
SINGLE-CRYSTAL - 2	6.9 ± 0.3	4.4 ± 0.0
POLYCRYSTALLINE - 1	3.4 ± 0.7	0.3 ± 0.0
POLYCRYSTALLINE - 2	3.4 ± 0.2	0.5 ± 0.2

factor of two, the polycrystalline silicon samples decreased by more than a factor of five. The change in the photoconductivity decay time of the single-crystal samples, heat-treated at 1000°C for 25 hours in flowing nitrogen, is small enough (less than a factor of two) that the minority-carrier lifetime is probably not being degraded by diffusion of impurities from the diffusion furnace. The change in the photoconductivity decay time of the polycrystalline silicn, by more than a factor of five, is significant and could be due to a number of factors.

The next experiment was performed to evaluate the effect of wafer thickness and time at 1000°C on the degradation of the minority carrier lifetime. Several 10cm x 10cm polycrystalline silicon wafers were selected from one section of Semix brick C4-87E. This material was cut from the central portion of an ingot in order to obtain wafers that were symmetrical about the center. The wafers, which were quartered into 5cm x 5cm samples, were etched to thicknesses of 200, 250, 300, and 350 microns using a CP-type etch. Each quarter wafer was sand-blasted on the back side only using 320 mesh aluminum oxide powder in order to introduce damage. Each quarter wafer was paired with a 5cm x 5cm single-crystal silicon wafer of the same thickness which was also damaged on the back side.

The polycrystalline and single-crystal silicon quarter wafers were assembled into four groups which consisted of one polycrystalline and one single-crystal silicon wafer of each thickness. One group, the control group, was not heat-treated. The remaining three groups were heat-treated for either 1, 5, or 25 hours.

Heat treatments took place under flowing nitrogen at 1000°C in a fused quartz tube furnace. After heat-treatment the wafers were CP-etched to remove any surface damage and then lightly diffused in order to measure the microwave photoconductivity decay time constant. After these measurements were completed, the wafers were used to fabricate $4cm^2$ solar cells, and the light I-V characteristics were evaluated.

The results of these measurements were ambiguous. The variation of the photoconductivity decay time with wafer thickness and anneal time at 1000°C in nitrogen for the single-crystal and polycrystalline silicon wafers is shown in Tables 3 and 4, respectively. There was no systematic degradation with anneal time in any of the single-crystal samples, although those samples heat-treated for 25 hours did have somewhat lower values of photoconductivity decay time. However, the photoconductivity decay time, and therefore the minority carrier lifetime, of the polycrystalline silicon wafers did decrease with anneal time for all thicknesses. The photoconductivity decay time was degraded

TABLE 3

Change in photoconductivity decay time for single-crystal silicon samples heat-treated at 1000°C in nitrogen.

NOMINAL THICKNESS (MICRONS)	ANNEAL TIME (HOURS)	SAMPLE SIZE	PULSE HEIGHT (mV)	PHOTOCONDUCTIVITY DECAY TIME (μsec)
200	0	8	87 (5)	6.8 (0.3)
	1	8	134 (9)	6.3 (0.9)
	5	8	138 (5)	7.6 (0.6)
	25	8	137 (5)	4.3 (0.4)
250	0	0	-	-
	1	8	108 (6)	6.4 (0.9)
	5	8	105 (4)	6.0 (0.9)
	25	8	103 (5)	3.4 (0.2)
300	0	3	115 (5)	4.8 (0.5)
	1	8	79 (2)	4.7 (0.3)
	5	8	71 (2)	5.7 (0.8)
	25	8	68 (7)	3.3 (0.2)
350	0	8	85 (4)	6.9 (0.2)
	1	8	61 (2)	5.1 (0.6)
	5	8	59 (2)	3.1 (0.2)
	25	8	58 (1)	3.0 (0.0)

Average (Standard Deviation)

TABLE 4

Change in photoconductivity decay time for polycrystalline silicon samples heat-treated at 1000°C in nitrogen.

NOMINAL THICKNESS (MICRONS)	ANNEAL TIME (HOURS)	SAMPLE SIZE	PULSE HEIGHT (mV)	PHOTOCONDUCTIVITY DECAY TIME (μsec)
200	0	4	101 (5)	2.6 (0.2)
	1	8	144 (17)	2.6 (0.4)
	5	8	131 (19)	1.0 (0.3)
	25	8	52 (6)	0.4 (0.1)
250	0	8	87 (3)	3.4 (0.4)
	1	8	108 (4)	2.9 (0.5)
	5	8	90 (16)	1.1 (0.4)
	25	8	84 (11)	0.7 (0.1)
300	0	8	63 (4)	4.1 (0.7)
	1	8	64 (5)	1.9 (0.2)
	5	8	64 (6)	1.4 (0.5)
	25	8	57 (4)	0.5 (0.1)
350	0	8	45 (1)	4.1 (0.3)
	1	8	53 (2)	3.6 (0.0)
	5	8	62 (7)	1.4 (0.8)
	25	8	63 (4)	0.8 (0.0)

Average (Standard Deviation)

by more than a factor of five after 25 hours at 1000°C in flowing nitrogen. While the photoconductivity decay time of the single-crystal samples also decreased, it was typically by less than 50 pecent, similar to the previous experiments. These results seem to indicate that minority carrier lifetime-killing impurities, if present in this polycrystalline silicon, are not being gettered by this particular heat treatment, and implies that there is a mechanism, activated by high temperatures in this particular nitrogen environment, which degrades the minority carrier lifetime of polycrystalline silicon significantly more than that of single-crystal silicon.

These conclusions were <u>not</u> confirmed by the electrical measurements of the $4cm^2$ solar cells fabricated from the heat-treated wafers. The results initially seemed to indicate that gettering was occurring. However, the characteristics of the <u>unannealed</u> samples were very poor when compared to the results of cells previously fabricated from Semix material for the thickness-resistivity matrix. In addition, the surface of the heat-treated cells was textured during processing, which could account for an improved short-circuit current density. We therefore disallowed the electrical results on the basis that the I-V characteristics were probably not truly representative of the material or the gettering process.

Because no satisfactory solar cells were fabricated, this experiment was repeated, except that only one wafer thickness was used. An additional five wafers from the same section of Semix brick C4-87E were quartered and thinned using a CP-type etch to a nominal thickness of 300 $\pm$ 10 microns. Each quarter wafer was sand-blasted on the back side only using 320 mesh aluminum oxide powder in order to introduce damage. Each quarter was paired with a 5cm x 5cm single-crystal wafer (ostensibly serial wafers from one ingot) of the same thickness that was also damaged on the back side.

Groups of polycrystalline and single-crystal wafers were heat-treated for 1, 5 and 25 hours at 1000^{o}C in flowing nitrogen. One group, the controls, was not heat-treated. After the heat-treatments were completed, all wafers, including the controls, were CP-etched to remove any surface damage, and then lightly diffused in order to measure the photoconductivity decay time constant. Tables 5 and 6 summarize this data for the single-crystal and polycrystalline wafers, respectively.

For the single-crystal monitor wafers, shown in Table 5, the pulse height (relative sheet resistivity modulation due to the photogeneration of carriers), which is sensitive to resistivity (dopant concentration) [4], is constant. The photoconductivity decay time, in four out of five cases, is significantly lower after 5 hours at 1000^{o}C. The wafers that

TABLE 5

Change in photoconductivity decay time for single-crystal silicon samples heat-treated at 1000°C in nitrogen.

WAFER NUMBER	ANNEAL TIME (HOURS)	SAMPLE SIZE	PULSE HEIGHT (mV)	PHOTOCONDUCTIVITY DECAY TIME (μsec)
1	0	8	62 (4)	21.1 (0.5)
	1	8	58 (5)	18.7 (0.4)
	5	8	56 (4)	18.4 (0.7)
	25	8	58 (4)	20.1 (1.0)
2	0	8	64 (3)	21.3 (0.5)
	1	8	58 (4)	13.4 (0.3)
	5	8	63 (3)	6.9 (0.5)
	25	8	57 (2)	11.4 (1.4)
3	0	8	65 (1)	22.3 (0.8)
	1	8	55 (2)	12.9 (0.3)
	5	8	59 (4)	6.5 (0.4)
	25	8	61 (2)	10.9 (1.0)
4	0	6	63 (3)	22.2 (0.5)
	1	8	59 (3)	16.8 (0.7)
	5	8	58 (2)	5.6 (0.6)
	25	8	60 (3)	11.0 (2.0)
5	0	8	63 (4)	22.8 (0.5)
	1	8	60 (4)	17.1 (0.4)
	5	8	61 (3)	9.0 (1.1)
	25	8	61 (3)	11.5 (2.0)

Average (Standard Deviation)

were not heat-treated always had the longest photoconductivity decay time constant and the least scatter, less than 5 percent. The wafers that were annealed for 25 hours had the most scatter, about 10 to 20 percent. These results would indicate that the damage gettering heat treatment up to 5 hours tends to decrease the minority carrier lifetime with time at 1000°C; annealing for 25 hours tends to improve the minority carrier lifetime, but does not restore the original value. The resistivity is not significantly influenced by the heat-treatments.

In contrast, results for the polycrystalline wafers, shown in Table 6, indicate that the majority carrier concentration may be modified by the heat-treatment, since the pulse height decreases with time at 1000°C. In addition, the photoconductivity decay time decreases significantly with time at 1000°C, which implies that the minority carrier lifetime is being substantially reduced by the heat-treatments. The scatter in the data shows no trends; unlike the single-crystal monitor wafers, the photoconductivity decay time is not improved by heat-treatments for 25 hours; it is less than the photoconductivity decay time after 5 hours at 1000°C. As in the previous experiments, the photoconductivity decay time is seen to be degraded by a factor of 5 to 10 due to the 1000°C heat-treatment for 25 hours.

TABLE 6

Change in photoconductivity decay time for polycrystalline silicon samples heat-treated at 1000°C in nitrogen.

WAFER NUMBER	ANNEAL TIME (HOURS)	SAMPLE SIZE	PULSE HEIGHT (mV)	PHOTOCONDUCTIVITY DECAY TIME (μsec)
27	0	7	73 (3)	4.1 (0.4)
	1	8	75 (4)	4.4 (0.9)
	5	8	55 (6)	3.3 (1.0)
	25	8	47 (4)	0.9 (0.1)
31	0	8	62 (3)	4.2 (0.5)
	1	8	59 (4)	3.8 (0.5)
	5	8	30 (4)	2.7 (0.4)
	25	8	44 (6)	0.8 (0.1)
36	0	8	76 (5)	6.3 (0.9)
	1	8	67 (3)	3.8 (0.3)
	5	8	54 (9)	2.9 (0.7)
	25	8	42 (9)	1.3 (0.5)
42	0	8	67 (4)	6.8 (1.3)
	1	8	57 (2)	4.2 (0.3)
	5	8	54 (5)	2.6 (0.4)
	25	8	39 (8)	1.2 (0.6)
45	0	8	63 (5)	7.9 (1.6)
	1	8	59 (4)	5.1 (0.6)
	5	8	57 (4)	3.6 (0.8)
	25	8	41 (4)	0.7 (0.1)

Average (Standard Deviation)

All of these results indicate that these damage-gettering heat treatments result in changes in cast polycrystalline silicon that are very different from those seen in single-crystal Czochralski silicon. The effect of these changes in the electrical performance will be evaluted by measuring $4cm^2$ solar cells fabricated with these wafers using a high efficiency process [5]. Particular attention has been focused on avoiding any process that would result in a textured surface, which would tend to enhance the light-generated current. The results will be reported in the following quarter.

B. Hydrogenation - Hydrogen Passivation

A number of recent reports indicate that monatomic hydrogen can be successfully used to substantially improve the open-circuit voltage, fill-factor, and efficiency of polycrystalline silicon solar cells fabricated from silicon-on-ceramic (SOC) [6], upgraded metallurgical grade (UMG) silicon [7], and edge-defined film-fed growth (EFG) silicon [8]. The hydrogen appears to be bound in the grain boundaries [9], and is believed to reduce grain boundary minority carrier recombination by eliminating grain boundary trappping states due to dangling bonds. A useful process for the hydrogenation of cast poly-crystalline silicon has not been established.

The open-circuit voltage of the cells fabricated for the thickness-resistivity matrix showed a large degree of scatter and, in some cases, very low values, even though the fill factor was better than 70 percent. The cause of this behavior is currently being investigated with the mini-cell work, but it may be due to excessive recombination in the space-charge region at the grain and subgrain boundaries. If this is indeed the case, and if hydrogenation does result in the effective reduction or elimination of this recombination, then this process may yield a substantial improvement in those cells with low values of open-circuit voltage.

The effect of hydrogen passivation on the performance of large-grain polycrystalline silicon will first be investigated by hydrogenating solar cells using a DC plasma technique. Work this month consisted of refurbishing an existing system in which to perform the hydrogenation. The system consists of a vacuum system with steel bell jar capable of a final pessure of 10^{-6} Torr, a gas system for introducing hydrogen gas into the chamber, and a high voltage power supply for creating the plasma.

Samples will be heated with a 1" x 1" high purity ceramic heater. The system will be completed and preliminary experiments will begin after the addition of a temperature controller during the next quarter.

IV. CONCLUSIONS

Analysis of the thickness-resistivity matrix during the previous quarter indicated that the open-circuit voltage and the fill-factor of the $4cm^2$ solar cells fabricated from large-grain (grain diameter greater than 1 to 2 mm) polycrystalline silicon had substantial amounts of scatter which were not related to the main experimental variables - thickness or bulk resistivity. Therefore, the spatial nature of the degradation in open-circuit voltage and fill-factor was investigated by fabricating and testing an array of small photodiodes (mini-cells) across several 10cm x 10cm wafers.

Work during this quarter consisted of measuring the light I-V characteristics of the mini-cell wafer set and determining the average characteristics for each wafer. Although the average open-circuit voltage of the polycrystalline cells is always less than that of the cells from the single-crystal Czochralski control wafer, the scatter for four of the six polycrystalline silicon wafers is the same. The average and scatter of the fill-factor for these wafers is also the same as that of the single-crystal controls. However, two of the polycrystalline silicon wafers have values of open-circuit voltages and fill-factor that vary widely across the wafer. The wafers also have significantly degraded averages of open-circuit voltage and fill-factor when compared to either the single-

crystal or the other polycrystalline silicon wafers. In addition, these wafers have many cells whose shunt conductance is greater than 10 mmho/cm^2. Microscopic examination showed that many inclusions are present in these wafers, which implies that, to some extent, the scatter in the open-circuit voltage, fill-factor, and peak-power of cells presently fabricated from cast large-grain polycrystalline silicon is due to inclusions, which act as resistive shunts. However, since other wafers have cells whose average shunt conductance is consistently below 1 mmho/cm^2, and which have no indication of inclusions, this defect is not intrinsic to this polycrystalline silicon material or to the casting process.

The results of the earlier thickness-resistivity matrix indicated that the light-generated current in large-grain polycrystalline silicon is dominated by recombination of photogenerated carriers in the grain volumes, as opposed to recombination at the grain boundaries. This conclusion is confirmed by the results from the mini-cell wafers. The short-circuit current density is 97 percent of that of the single-crystal Czochralski wafer in the best case. For the worst case, it is about 14 percent lower. The scatter in the short-circuit current density is typically less than 3 percent; in the worst case, it is only about 7 percent.

Since the limiting mechanism of light-generated current is in the bulk, improvements will follow if the sources of recombination in the bulk are eliminated. Several experiments were performed to evaluate the usefulness of a 1000°C back-side damage-gettering heat-treatment for removing minority-carrier lifetime-killing impurities from the bulk. At present, no improvement in minority-carrier lifetime has been observed. The photoconductivity decay time constant, which is related to the minority-carrier lifetime, is systematically and significantly degraded by longer heat treatments at 1000°C in flowing nitrogen. There appears to be a minority-carrier lifetime-killing mechanism, specific to large-grain polycrystalline silicon, that is activated by the high temperatures present in the particular damage-gettering heat treatments that were used.

REFERENCES

1. J. Culik, "Process Research on Polycrystalline Silicon Material (PROPSM)", JPL Contract No. 955902, 9th Quarterly Technical Report (January-March, 1983).

2. T. Saitoh, T. Warabisako, E. Kuroda, H. Itoh, S. Matsubara, and T. Tokuyama, "Impurity Gettering of Polycrystalline Solar Cells Fabricated From Refined Metallurgical-Grade Silicon", IEEE Tran. Electron Dev. ED-27, 671 (1980).

3. S.M. Johnson and J.S. Culik, "The Measurement of Variations in Minority Carrier Lifetime Due to Microstructural Defects in Large Area Polysilicon Wafers", Proc. 16th IEEE Photovoltaic Specialists Conf., 548 (1982).

4. J. Culik, "Determination of the Bulk Resistivity of Polycrystalline Silicon Wafers Using a Contactless Microwave Reflection Technique", Proc. 15th IEEE Photovoltaic Specialists Conf., 1170 (1981).

5. G. Storti, J. Culik, and C. Wrigley, "Development of a High Efficiency Thin Silicon Solar Cell", Final Report, JPL Contract No. 954883, December 1980.

6. C.H. Seager, D.S. Ginley, and J.D. Zook, "Improvements of Polycrystalline Silicon Solar Cells With Grain-Boundary Hydrogenation Techniques", App. Phys. Lett., 36, 831 (1980).

7. P.H. Robinson and R.V. D'Aiello, "The Effect of Atomic Hydrogen Passivation on Polycrystalline Silicon Epitaxial Solar Cells", App. Phys. Lett., 39, 63 (1981).

8. J.I. Hanoka, C.H. Seager, D.J. Sharp, and J.K.G. Panitz, "Hydrogen Passivation of Defects in Silicon Ribbon Grown by the Edge-Defined Film-Fed Growth Process", App. Phys. Lett., 42, 618 (1983).

9. D.S. Ginley and D.M. Haaland, "Observation of Grain Boundary Hydrogen in Polycrystalline Silicon with Fourier Transform Infrared Spectroscopy". App. Phys. Lett., 39, 271 (1981).

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APPENDIX

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MECHANISMS LIMITING PERFORMANCE IN POLYCRYSTALLINE SILICON SOLAR CELLS

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ABSTRACT

Performance-limiting mechanisms in polycrystalline silicon were investigated by fabricating a matrix of 4cm^2 solar cells of various thicknesses from 10cm x 10cm polycrystalline silicon wafers of several bulk resistivities. The analysis of the results of this matrix indicates that bulk recombination is the dominant factor limiting the short-circuit current in large-grain (greater than 1 to 2 mm in diameter) polycrystalline silicon, the same mechanism that limits the short-circuit current in single-crystal silicon. The average open-circuit voltage of the polycrystalline cells is 30 to 70 mV lower than that of the single-crystal (control) cells; the fill-factor is comparable. Both open-circuit voltage and fill-factor have substantial scatter which is not related to thickness or resistivity. This implies that these parameters are sensitive to an additional mechanism which is probably spatial in nature since the cell position on the wafer was not controlled.

1. Introduction

Over the past several years, a number of forms of polycrystalline silicon material have become available for use in fabricating photovoltaic devices. Whether sheet material cut from a cast ingot (Wacker Silso, Semix UCP, or Crystal Systems HEM) or ribbon material (Westinghouse WEB, Mobil EFG, or Solavolt RTR), all suffer to some extent from degradation of their performance, as compared to single-crystal silicon, when used to fabricate large-area (greater than 1 cm^2) solar cells (1-4). In most cases the performance-limiting mechanisms are assumed to be structurally-related, due to the polycrystalline nature of most of these materials. However, recent work has indicated that not all grain boundaries contribute to the performance degradation (5,6). Only those grain boundaries, and subgrain boundaries, which have a high dislocation content cause losses in performance (7,8).

The purpose of this work is to investigate the performance-limiting mechanisms in large-grain (greater than 1 to 2 mm in diameter) polycrystalline silicon. For solar cells fabricated from single-crystal silicon, the short-circuit current is sensitive to thickness and to minority carrier diffusion length, which tends to decrease as the resistivity decreases. The open-circuit voltage and the fill-factor of solar cells with a back surface field are relatively insensitive to thickness. However, the open-circuit voltage will increase as the base resistivity decreases (9). These relationships in large-grain polycrystalline silicon were tested by fabricating a statistically significant number of $4cm^2$ solar cells from a selection of 10cm x 10cm wafers which had various resistivities and thicknesses. The performance of these polycrystalline cells was compared to that of co-processed single-crystal control cells of similar thickness and resistivity in order to determine the loss mechanisms that are unique to polycrystalline silicon.

2. Experimental

The performance-limiting mechanisms in polycrystalline silicon were investigated by fabricating a matrix of $4cm^2$ solar cells of various thicknesses from polycrystalline P-type silicon wafers of several resistivities as supplied by Semix, Inc.

A high-efficiency process was used to fabricate the cells; the process sequence is shown in Figure 1 (10). The wafers were thinned to the nominal thickness - 100, 150, 200, 250 and 300 microns - using a CP-type etch; then diffused with phosphorus to form a thin N^+ layer and junction on both sides. The nominal surface resistivity was 70 ohms/□. The rear junction was compensated by aluminum alloy to form a thick P^+ back surface field (BSF). Front and rear contacts were Ti/Pd/Ag; the front pattern was defined photolithographically. Finally, the wafers were sawn into 2cm x 2cm cells, and a Ta_2O_5 anti-reflection coating was applied. For each group of wafers, single-crystal control wafers of similar thickness and resistivity were included to monitor the process.

The current-voltage (I-V) characteristics - short-circuit current, open-circuit voltage, maximum power, and fill-factor - of all solar cells were measured under AM0, 135 mW/cm^2, 25°C conditions.

3. Results and Discussion

Table 1 shows the number of $4cm^2$ polycrystalline solar cells for each thickness and resistivity category by lot number. The resistivity of the polycrystalline silicon wafers fell into three ranges: "low resistivity", 0.5 to 0.6 ohm-cm; "medium resistivity", 1.0 to 1.9 ohm-cm; and "high resistivity", 4.2 to 6.5 ohm-cm.

The variation of short-circuit current with thickness and resistivity is shown in Table 2. The short-circuit current of the polycrystalline cells decreases as the resistivity decreases, just as it does with single-crystal (control) cells, as shown in Table 3. The dependence of the short-circuit current of the single-crystal cells on resistivity is attributed to the dependence of the minority carrier diffusion length on the dopant concentration. This behavior, though not well understood, is at least well known for Czochralski single-crystal silicon (11,12,13). The variation of the short-circuit current of the single-crystal cells with base thickness is also related to minority carrier diffusion length. If the base width is less than the minority carrier diffusion length, then nearly all of the carriers that are photogenerated will be collected; as the base width increases, the amount of light absorbed and the short-circuit current also increase. The short-circuit current will continue to increase with cell thickness until the base width is approximately equal to the minority carrier diffusion length. When the base width is greater than the minority carrier diffusion length, even though additional carriers may be generated deeper in the bulk they will not be collected. Therefore, at some base thickness approximately equal to the minority carrier diffusion length, the short-circuit will saturate. This current saturation is clearly seen for the single-crystal (control) cells. For each lot of wafers, the short-circuit current increases with cell thickness until it saturates. As the resistivity increases, and therefore the minority-carrier diffusion length increases, the cell thickness at which the short-circuit current saturates also increases. This behavior, though less clearly seen, is nevertheless also present for the polycrystalline cells. However, the short-circuit current of all polycrystalline cells appears to have saturated for cell thicknesses greater than 150 microns. This fact, together with the short-circuit currents for the polycrystalline cells being five to ten percent lower than those of single crystal cells of similar resistivity, indicates that the minority carrier diffusion length of the polycrystalline material is less than that of the single-crystal silicon wafers.

It does not appear that the reduced short-circuit currents are the result of recombination at the grain boundaries. If this were the case, then there should be even more scatter in the data since no attempt was made to control the grain size, which varied from about 1 to 10 mm in diameter. With the exception of the cells from Lot 1, the scatter in the short-circuit current of the polycrystalline cells is equivalent to that of the single-crystal control cells, that is, three to four percent. This result is consistent with the previous work - both theoretical and experimental - which shows that the light-generated current is not substantially affected by recombination at the grain boundaries when the grain diameter is several times larger than the minority carrier diffusion length (14,15). For a diffusion length of 100 to 150 microns, as indicated by the behavior of the short-circuit current with thickness and resistivity, this dimension would be on the order of 1 to 2 mm. In most present examples of cast

polycrystalline silicon (Semix, Wacker, HEM) the grain size is consistently equal to or greater than this dimension. Hence, the short-circuit current of these materials should be dominated by bulk properties, rather than grain boundary recombination. This also implies that forming polycrystalline silicon with grain diameters larger than several minority carrier diffusion lengths will not result in any substantial increase in short-circuit current. Improvements in the short-circuit current of large-grain polycrystalline silicon, at most five to ten percent, will be mainly due to elimination of the sources of recombination in the bulk.

The results for the open-circuit voltage of the polycrystalline cells in the thickness-resistivity matrix are shown in Table 4. Although there is some indication that the open-circuit voltage increases as the resistivity decreases, it is very difficult to conclude that dopant concentration is the dominant factor because the scatter in the data ranges from less than one percent to more than twelve percent. Likewise, it is difficult to establish any clear dependence of open-circuit voltage on thickness, though in some lots the thinner cells did have slightly higher values of open-circuit voltage.

For comparison, Table 5 gives the results of the open-circuit voltage of the single-crystal (control) cells. As expected, the open-circuit voltage increases as the resistivity decreases and, because of the back surface field, is not very sensitive to thickness. The average open-circuit voltage of the single-crystal cells is 30 to 70 mV greater than that of the polycrystalline cells in the same thickness-resistivity category. For most single-crystal control groups the scatter is within 10 mV of the mean, that is, less than two percent. In the worst case the scatter is about five percent of the mean. Hence, the scatter in the open-circuit voltage of the polycrystalline cells is significantly greater than that of the single-crystal (control) cells.

Most of the thickness-resistivity groups of polycrystalline cells which showed very large amounts of open-circuit voltage scatter also had a very high average shunt conductance, as shown by the shunt conductance data in Table 6. In these groups the low open-circuit voltage, and also the scatter, were most likely the direct result of excessive shunt conductance. However, one group, the 150 micron thick cells of Lot 2, had shunt conductances which could in no way account for the low average or the scatter in the open-circuit voltage. In addition, polycrystalline cells with moderate amounts of open-circuit voltage scatter ($\pm$5 to $\pm$20 mV) invariably had shunt conductances that were so low as to have no significant effect on the open-circuit voltage.

The low average open-circuit voltage (30 to 70 mV lower than single-crystal control cells) and the scatter in the open-circuit voltages of the non-shunted polycrystalline cells appears to indicate that there is a voltage-controlling mechanism, not present in the single-crystal (control) cells, which is limiting the open-circuit voltage.

A comparison of the fill-factor of the polycrystalline cells to that of the single-crystal (control) cells is shown in Table 7. As with the open-circuit voltage, most of the groups with large amounts of scatter were also badly shunted; the shunts were very likely the cause of the low fill-factors as well as the low open-circuit voltages. The average fill-factor of most of the groups of non-shunted polycrystalline cells were not significantly different from that of the single-crystal (control) cells. However, the fill-factor of four polycrystalline groups (Lot 6 - 250 microns; Lot 2- 150 microns; and Lot 3 - 150 and 200 microns) was much lower than that of their single-crystal controls, and not because of shunting. This indicates that, while there does not appear to be any fundamental limit to fill-factor in large-grain polycrystalline silicon, there is a mechanism, not present in single crystal silicon, which can reduce the fill-factor in some polycrystalline samples.

4. Conclusions

Analysis of the results of the thickness-resistivity matrix indicates that the short-circuit current of large-grain (greater than 1 to 2 mm in diameter) polycrystalline silicon is dominated by recombination of photogenerated minority carriers in the bulk, as opposed to recombination at the grain boundaries. This result is in agreement with previous theoretical and experimental results which indicate that the light-generated current is not substantially affected by recombination at the grain boundaries when the grain diameter is several times larger than the minority carrier diffusion length. However, it also implies that significant improvements in the short-circuit current of large-grain polycrystalline silicon will be mainly due to elimination of sources of recombination in the bulk.

Both the open-circuit voltage and fill-factor of the polycrystalline solar cells in the thickness-resistivity matrix had substantial amounts of scatter which were not related to the main experimental variables - thickness and bulk resistivity. The scatter in the values of open-circuit voltage and fill-factor implies that there is an additional performance-limiting mechanism which may not be strongly associated with bulk properties. The degradation of these parameters appears to have a spatial nature and to be related to the grain structure since the grain boundary content of any particular cell on a wafer was not controlled.

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REFERENCES

1. H. I. Yoo and P. A. Iles, "Evaluation of Various Silicon Sheet Forms For Terrestrial Solar Cells", Proc. Symposia on Electronic and Optical Properties of Polycrystalline or Impure Semiconductors and Novel Silicon Growth Methods, 80-5, (ed. K. V. Ravi and B. O'Mara, Electrochemical Society, 1980), 57.

2. H. I. Yoo, P. A. Iles, D. C. Leung, and S. Hyland, "Improved Performance From Solar Cells Made From Candidate Sheet Silicon Material", Proc. 15th IEEE Photovoltaic Specialists Conf. (1981), 598.

3. J. A. Minahan, E. Castorena, and D. J. Dionne, "Solar Cells Fabricated With Unconventional Silicon Materials", Proc. 15th IEEE Photovoltaic Specialsts Conf. (1981), 608.

4. S. Hyland, P. Iles, D. Leung, G. Schwuttke, and J. A. A. Engelbrecht, "Interaction Between Cast Silcion Properties and Solar Cell Performance", Proc. 16th IEEE Photovoltaic Specialists Conf. (1982), 68.

5. B. L. Sopori, "The Influence of Defects on Solar Cell Parameters - An Experimental Study", Proc. Symposia on Electronic and Optical Properties of Polycrystalline or Impure Semiconductors and Novel Silicon Growth Methods, 80-5 (eds. K. V. Ravi and B. O'Mara, Electrochemical Society, 1980) 66.

6. S. M. Johnson, R. G. Rosemeier, C. D. Wang, R. W. Armstrong, H. C. Lin, and G. M. Storti, "Crystallographic Structure Effects on the Electrical Properties of Polycrystalline Solar Cells", Tech. Digest International Electron Devices Meeting (1980), 202.

7. W. F. Regnault, K. C. Yoo, S. M. Johnson, G. Breidenthal, R. G. Rosemeier, C. D. Wang, R. W. Armstrong, and H. C. Lin, "Investigation of the Microstructure and Photovoltaic Properties of Semicrystalline Silicon", Proc. 3rd Symposium on Materials and New Processing Technologies for Photovoltaics, 82-8, (eds. J. P. Dismukes, P. Rai-Cloudhury, E. Sirth, and L. P. Hunt, Electrochemical Society, 1982), 249.

8. S. M. Johnson and J. S. Culik, "The Measurement of Variations in Minority Carrier Lifetime Due to Microstructural Defects in Large Area Polysilicon Wafers", Proc. 16th Photovoltaic Specialists Conf. (1982), 548.

9. H. Hovel, Semiconductors and Semimetals, Vol. 11, Solar Cells (New York: Academic Press, 1975).

10. G. Storti, J. Culik, and C. Wrigley, "Development of a High Efficiency Thin Silicon Solar Cell", Final Report, JPL Contract No. 954883, December, 1980.

11. P. A. Iles and S. I. Soclof, "Effect of Impurity Doping Concentration on Solar Cell Output", Proc. 11th IEEE Photovoltaic Specialists Conf. (1975), 9.

12. B. Ross, "Survey of Literature on Minority Carrier Lifetimes in Silicon and Related Topics", Lifetime Factors in Silicon (ASTM STP 712), (ed. R. D. Westbrook, American Society for Testing and Materials 1980), 14.

13. C. Y. Wu and J. F. Chen, "Doping and Temperature Dependences of Minority- Carrier Diffusion Length and Lifetime Deduced for the Spectral Measurements of P-N Junction Solar Cells", Sol. St. Electr., 25:679 (1982).

14. A. Rothwarf, "Crystallite Size Considerations in Polycrystalline Solar Cells", Proc. 12th IEEE Photovoltaic Specialists Conf. (1976), 488.

15. G. M. Storti, S. M. Johnson, H. C. Lin, and C. D. Wang, "The Influence of Grains and Grain Boundaries on the Device Characteristics of Polycrystalline Silicon Solar Cells", Proc. 14th IEEE Photovoltaic Specialists Conf. (1980), 191.

FIGURE 1. THICKNESS-RESISTIVITY MATRIX TEST CELL PROCESS SEQUENCE

1.	Thinning Etch:	CP-type, final thicknesses: 100, 150, 200, 250, 300 microns.
2.	Diffusion:	Phosphine, tube diffusion; 70-80 ohms/□.
3.	BSF:	Englehard A-3484 aluminum paste, tube alloy, 30 seconds at 850°c; HCl post-alloy etch.
4.	Front Metallization:	Evaporated Ti/Pd contacts, photolithographically defined.
5.	Rear Metallization:	Evaporated Ti/Pd contacts.
6.	Electroplate Silver Conductor	
7.	AR Coating	Evaporated Ta_2O_5

Table 1. Sample size for $4cm^2$, polycrystalline silicon, AR-coated solar cells, by lot.

		THICKNESS (μM)					RESISTIVITY
	LOT NO.	100	150	200	250	300	(OHM-CM)
LOW RESISTIVITY	6		20	26	20		0.4 - 0.6
MEDIUM RESISTIVITY	1		6	20	19		1.3 - 1.7
	2		5	12	13	19	1.0 - 1.9
	7	9	14	11	8		1.2 - 1.8
HIGH RESISTIVITY	3	5	9	19			5.5 - 6.5
	5		10	18	22		4.2 - 6.2

NUMBER OF $4CM^2$, AR-COATED POLYCRYSTALLINE CELLS IN EACH THICKNESS-RESISTIVITY CATEGORY. BY LOT.

Table 2. Short-circuit current of polycrystalline silicon solar cells.

		THICKNESS (μM)				
	LOT NO.	100	150	200	250	300
LOW RESISTIVITY	6		126 (4)	127 (4)	127 (4)	
MEDIUM RESISTIVITY	1		132 (6)	128(16)	126(15)	
	2		132 (2)	127 (3)	135 (7)	131 (5)
	7	143 (2)	146 (2)	140 (3)	142 (2)	
HIGH RESISTIVITY	3	141 (3)	141 (2)	143 (2)		
	5		145 (4)	147 (5)	146 (6)	

MEAN (STANDARD DEVIATION ABOUT MEAN). IN mA. MEASURED AT AMO. 135 mW/CM^2. 25°C

Table 3. Short-circuit current of single-crystal silicon solar cells.

	THICKNESS (μM)					
	100	150	200	250	300	RESISTIVITY (OHM-CM)
LOW RESISTIVITY	145 (2)	149 (2)	148 (2)			0.7
	145 (1)	146 (2)	147 (3)	148 (2)		0.7
MEDIUM RESISTIVITY	154 (2)	159 (1)	155 (2)	159 (1)	159 (2)	1.7
		155 (2)	155 (4)	155 (1)		1.7
HIGH RESISTIVITY	153 (3)	159 (3)	162 (3)	164 (1)	163 (1)	7-22
	151 (4)	151 (2)	150 (3)			13-18
		156 (3)	164 (5)	161 (2)	159 (3)	10-16

MEAN (STANDARD DEVIATION ABOUT MEAN). IN mA. MEASURED AT AMO. 135 mW/CM^2

Table 4. Open-circuit voltage of polycrystalline silicon solar cells.

		THICKNESS (μM)				
	LOT NO.	100	150	200	250	300
LOW RESISTIVITY	6		577(24)	583 (8)	580 (8)	
MEDIUM RESISTIVITY	1		559 (5)	559(19)	559(14)	
	2		539(36)	538(67)	555(16)	553(11)
	7	587 (4)	586 (3)	573(10)	582 (4)	
HIGH RESISTIVITY	3	573 (8)	570 (4)	570 (5)		
	5		570(13)	552(30)	566(16)	

MEAN (STANDARD DEVIATION ABOUT MEAN), IN MV, MEASURED AT AMO, 135 MW/CM^2, 25°C

Table 5. Open-circuit voltage of single-crystal silicon solar cells.

	THICKNESS (μM)					
	100	150	200	250	300	RESISTIVITY (OHM-CM)
LOW RESISTIVITY	601 (4)	607 (4)	602 (5)			0.7
	607 (4)	612 (3)	612 (6)	609 (2)		0.7
MEDIUM RESISTIVITY	601 (8)	608 (2)	606 (3)	604 (3)	606 (1)	1.7
	606 (2)	559(10)	600 (9)	603 (3)		1.7
HIGH RESISTIVITY	580(15)	590 (5)	598 (3)	596 (4)	600 (3)	10-20
	598 (3)	599 (2)	593(26)			13-18
		602 (2)	607 (3)	601 (5)	590(15)	10-15

MEAN (STANDARD DEVIATION ABOUT MEAN), IN MV MEASURED AT AMO, 135 MW/CM^2, 25°C

Table 6. Shunt conductance of polycrystalline silicon solar cells.

		THICKNESS (μM)				
LOT NO.		100	150	200	250	300
LOW RESISTIVITY	6		19.7(41.5)	2.49(4.59)	3.31(3.74)	
MEDIUM RESISTIVITY	1		1.12(1.72)	7.59(4.58)	2.25(3.33)	
	2		2.47(2.11)	33.2(88.7)	26.5(51.6)	3.89(3.67)
	7	0.35(0.28)	0.56(0.58)	1.69(1.78)	0.99(1.00)	
HIGH RESISTIVITY	3	21.9(27.7)	5.58(5.16)	7.50(9.81)		
	5		4.31(6.63)	63.7(86.1)	0.56(1.23)	

MEAN (STANDARD DEVIATION ABOUT MEAN), IN MMHOS

Table 7. Comparison of the fill-factor of the polycrystalline and single-crystal silicon solar cells.

		THICKNESS (μM)				
	LOT NO.	100	150	200	250	300
LOW RESISTIVITY	6		68(11)*	73 (3)	71 (5)*	
			80 (1)	77 (6)	79 (1)	
MEDIUM RESISTIVITY	1		76 (2)	75 (2)	75 (4)	
			75 (1)	76 (1)	76 (1)	
	2		70(10)	70(14)	68(13)	74 (3)
			80 (1)	80 (1)	78 (2)	78 (1)
	7	76 (1)	76 (1)	75 (1)	76 (2)	
		76 (1)	77 (2)	78 (2)	79 (1)	
HIGH RESISTIVITY	3	70 (7)	64 (4)*	64 (4)*		
		75 (5)	78 (1)	77 (1)		
	5		75 (2)	64(15)	75 (1)	
			77 (1)	77 (3)	77 (3)	

POLYCRYSTALLINE MEAN [IN %], (STANDARD DEVIATION ABOUT MEAN [IN %])
SINGLE CRYSTAL MEAN [IN %], (STANDARD DEVIATION ABOUT MEAN [IN %])
MEASURED AT AMO, 135 MW/CM^2, 25°C